

atomera

Investor Presentation

March 2024

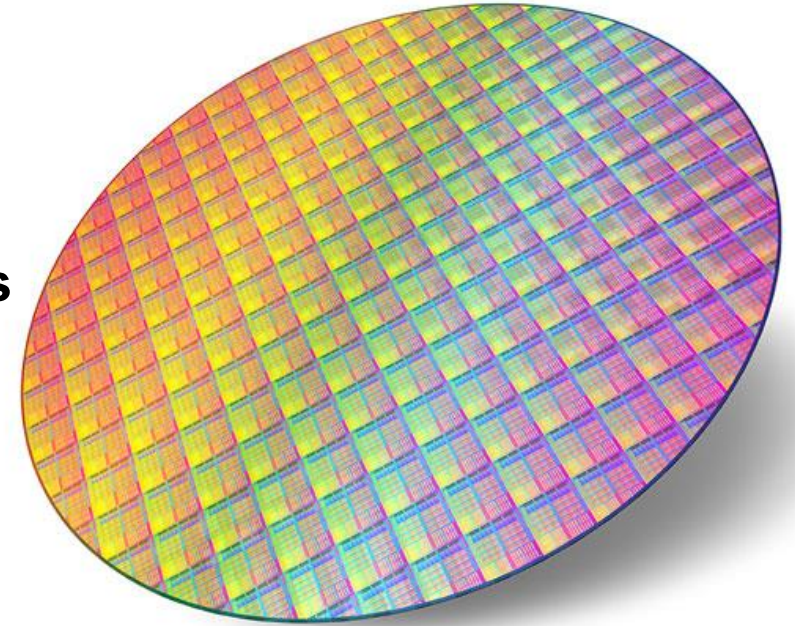
Safe Harbor



This presentation contains forward-looking statements concerning Atomera Incorporated (“Atomera,” the “Company,” “we,” “us,” and “our”). The words “believe,” “may,” “will,” “potentially,” “estimate,” “continue,” “anticipate,” “intend,” “could,” “would,” “project,” “plan,” “expect” and similar expressions that convey uncertainty of future events or outcomes are intended to identify forward-looking statements. These forward-looking statements are subject to a number of risks, uncertainties and assumptions, including those disclosed in the section "Risk Factors" included in our Annual Report on Form 10-K filed with the SEC on February 15, 2023 (the “Annual Report”) Quarterly Report on Form 10-Q filed with the SEC on November 1, 2023. In light of these risks, uncertainties and assumptions, the forward-looking events and circumstances discussed in this presentation may not occur and actual results could differ materially and adversely from those anticipated or implied in our forward-looking statements. You should not rely upon forward-looking statements as predictions of future events. Although we believe that the expectations reflected in our forward-looking statements are reasonable, we cannot guarantee that the future results, levels of activity, performance or events and circumstances described in the forward-looking statements will be achieved or occur.

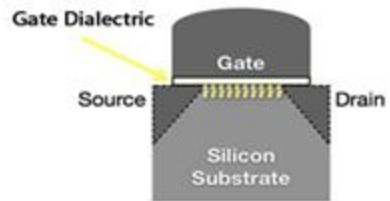
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- ▶ **Mears Silicon Technology (MST[®]) is a thin film used to enhance semiconductors**
 - Results in higher performance, lower power, and lower costs for ICs
- ▶ **Capital-light IP and technology licensing business**
- ▶ **Engaged with 50% of world's top semiconductor makers**
- ▶ **Licenses with five companies including two JDAs**
- ▶ **Strong team to commercialize technology**



Potential Benefits

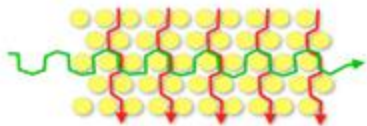
STANDARD SILICON TRANSISTOR



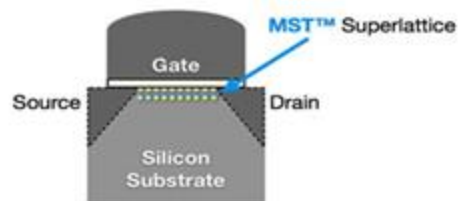
Standard Silicon Atomic Structure



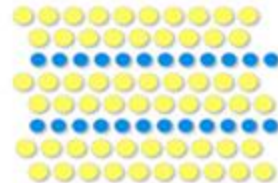
LIMITED Horizontal Current Flow +
EXCESSIVE Vertical Leakage



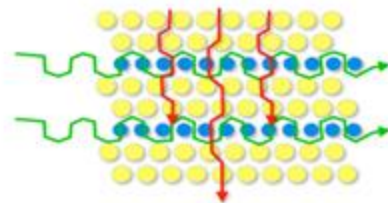
MST SILICON TRANSISTOR



MSTTM Silicon Atomic Structure



INCREASED Horizontal Current Flow +
REDUCED Vertical Leakage



► Improved Efficiency

- Higher transistor performance
- Lower power consumption
- Better reliability

► Lower cost

- Reduced die size
- Improved yield
- Higher throughput

► Same benefits as a node shrink

Target Customers & Partners



Integrated Device Manufacturers



Foundry



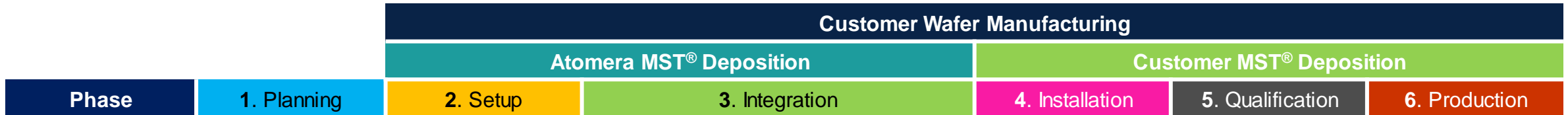
Fabless



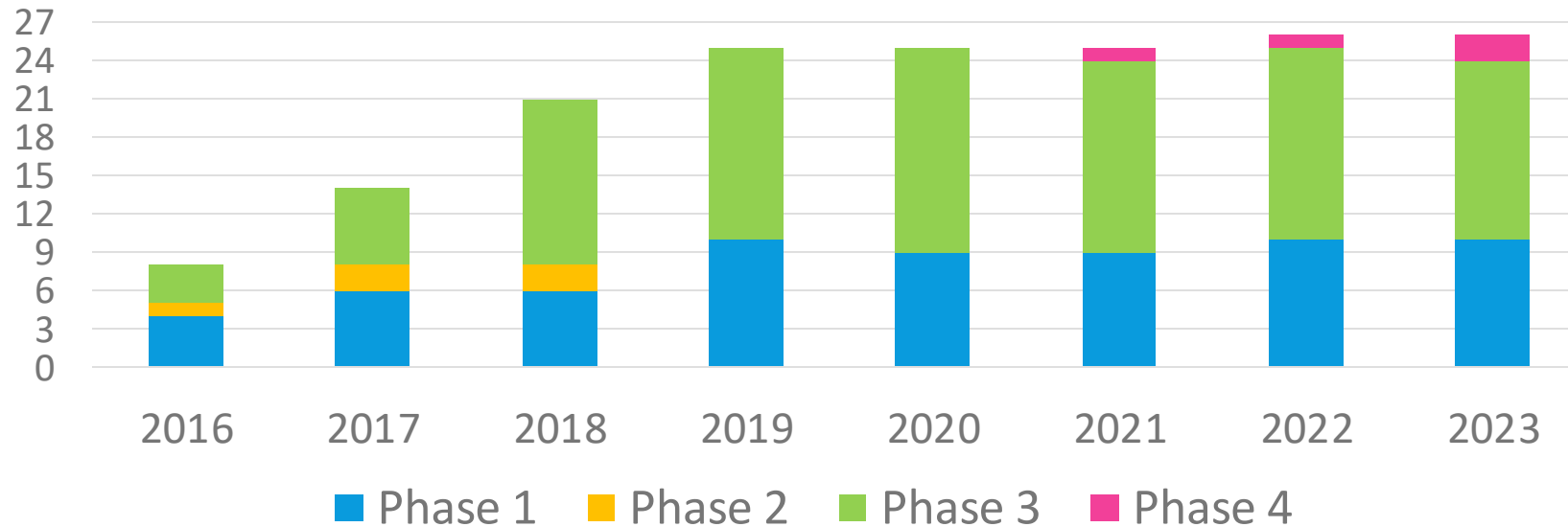
Tool Suppliers (Partners)



Customer Pipeline



Number of Customer Engagements

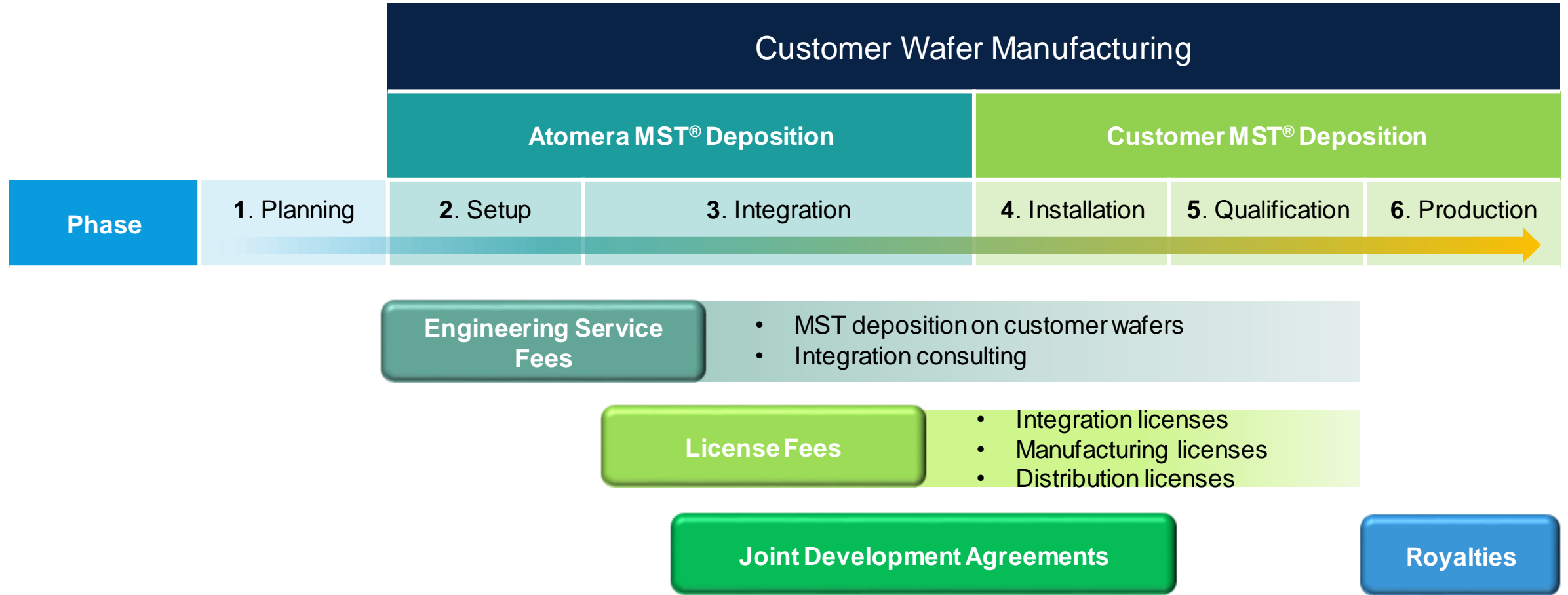


• 10 of the top 20 (IC Insights, McClean Report 2023)

^ End of year engagement count

- 20 customers, 26 engagements
- Working with 50% of the world's top semiconductor makers*

Customer Engagement & Revenue Model



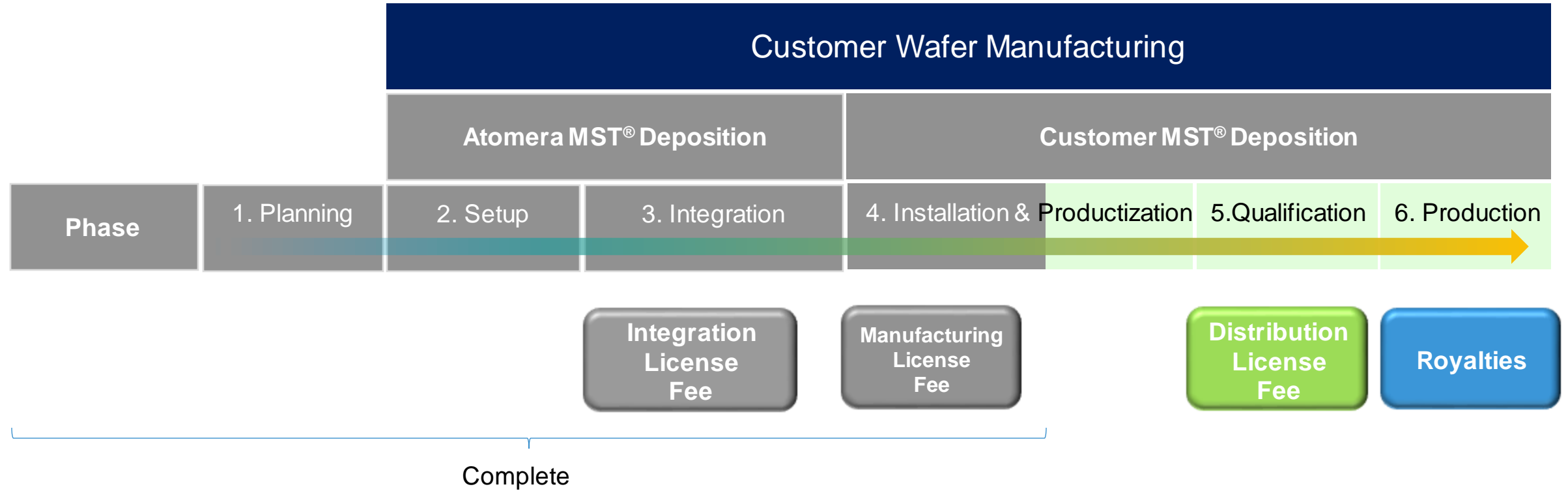


life.augmented

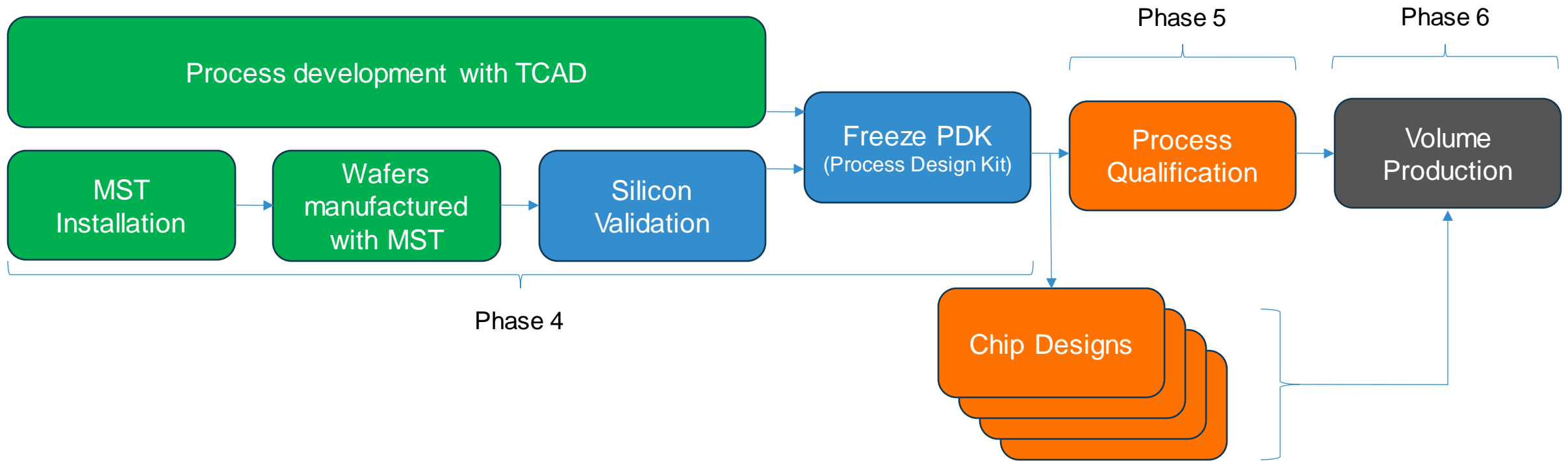


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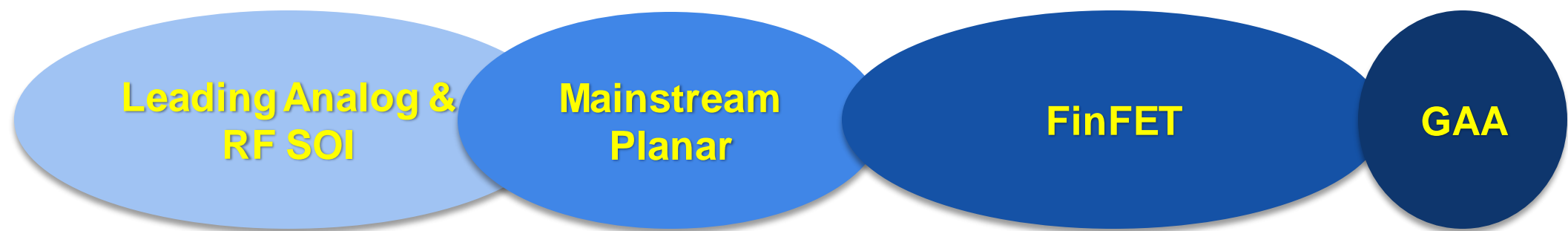
ST Path to Production



Productization cycle



MST Key Benefits Across Nodes



| | | | | | | | | | | | | |
|--------------------------------|-------|-------|------|------|------|------|------|---------|------|-----|-----|-----|
| Mobility | 8% | 20% | 25% | 10% | 15+% | | | | | | | |
| Dopant Engineering | 20% | 15% | 15% | 15% | 20% | | | | | | | |
| Reliability (TDDDB/BTI) | | 25% | 25% | 25% | 25% | | | | | | | |
| | 180nm | 130nm | 90nm | 65nm | 40nm | 28nm | 22nm | 16/14nm | 10nm | 7nm | 5nm | 2nm |

These Benefits are ADDITIVE & COMPLEMENTARY to other enhancement technologies





MST technology focus areas

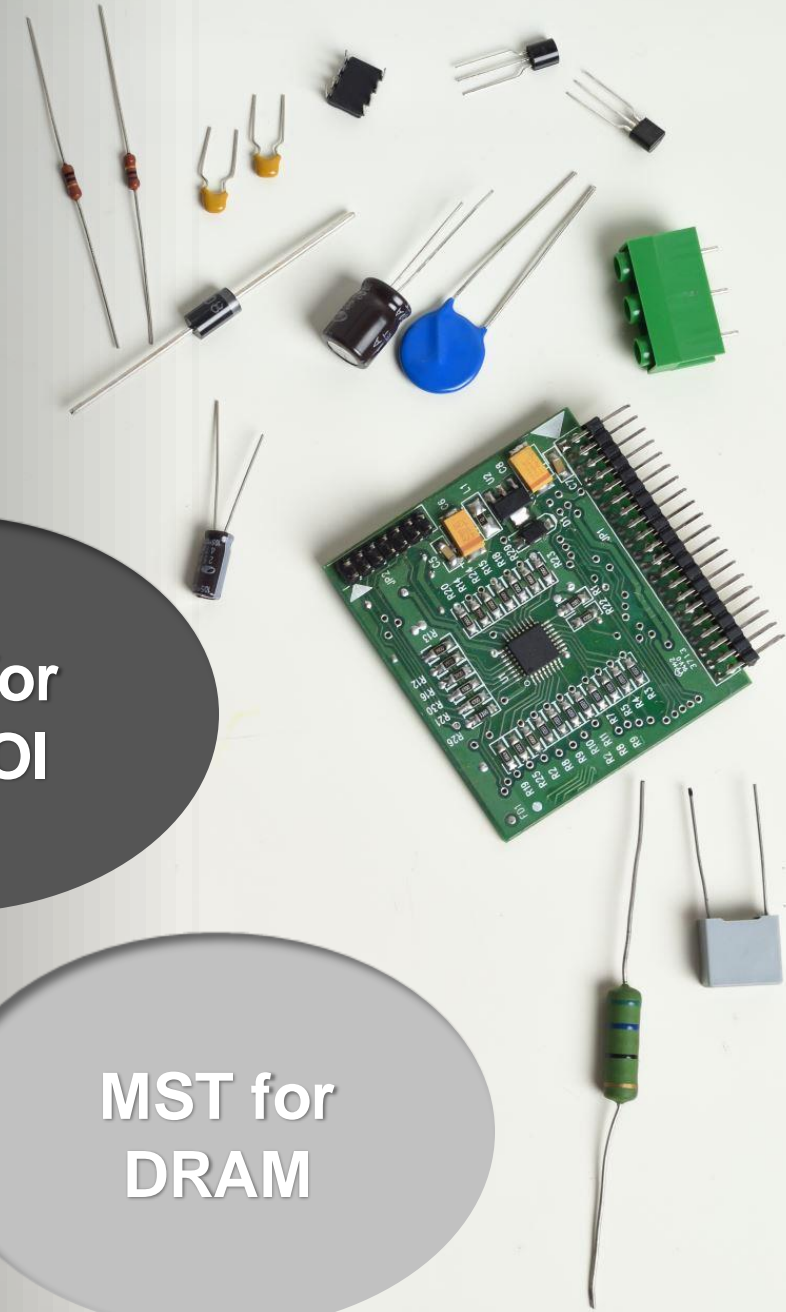


MST-SP,
SPX

MST for
RF-SOI

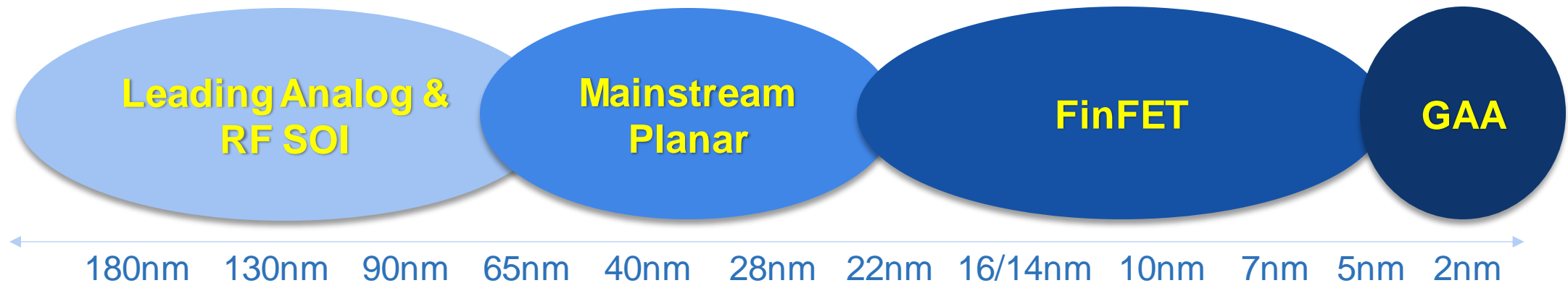
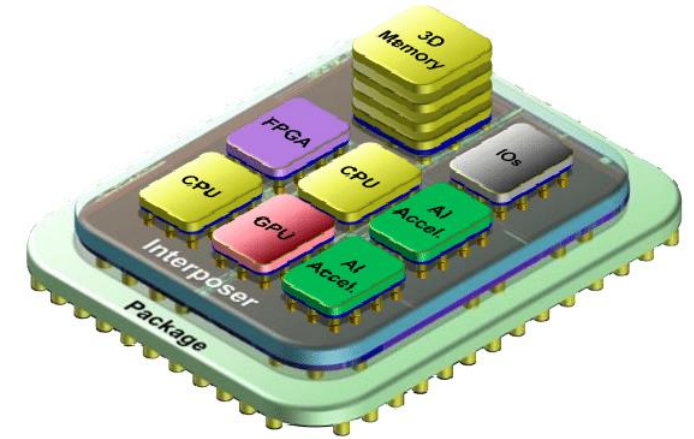
MST for
Advanced
Nodes

MST for
DRAM



MST optimizes AI performance

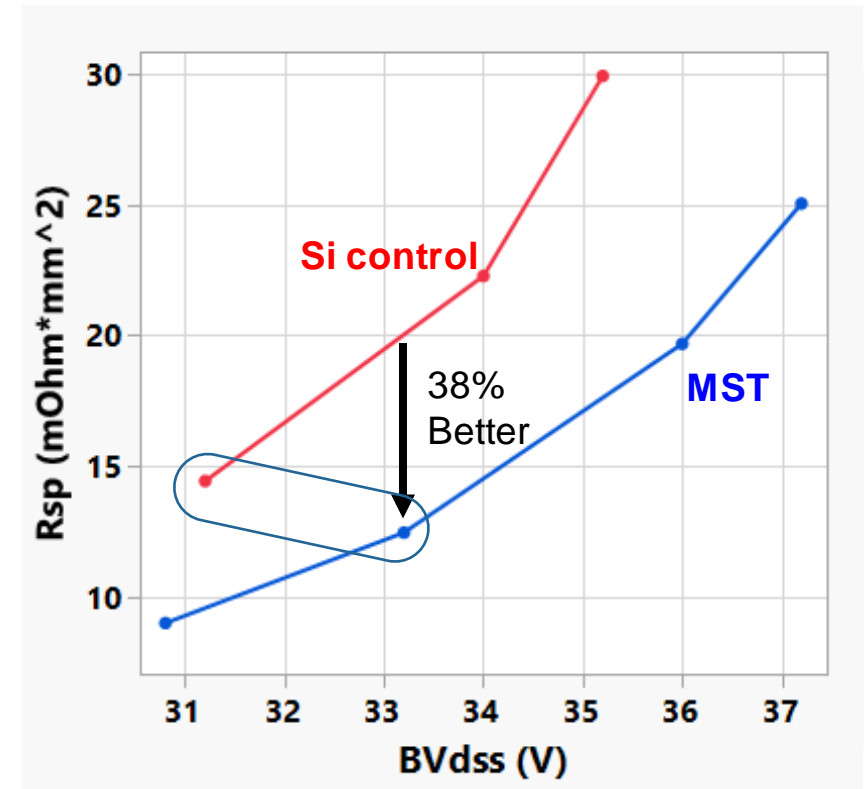
- ▶ **AI algorithms are driving unparalled computing demands**
 - Exceeding ideal single chip silicon area which impacts yield
- ▶ **Heterogenous chiplet architectures solve this problem**
- ▶ **Small chiplet designs can be optimized by process node**
- ▶ **MST's ability to enhance mature nodes brings great value**



MST-SPX targeting power devices



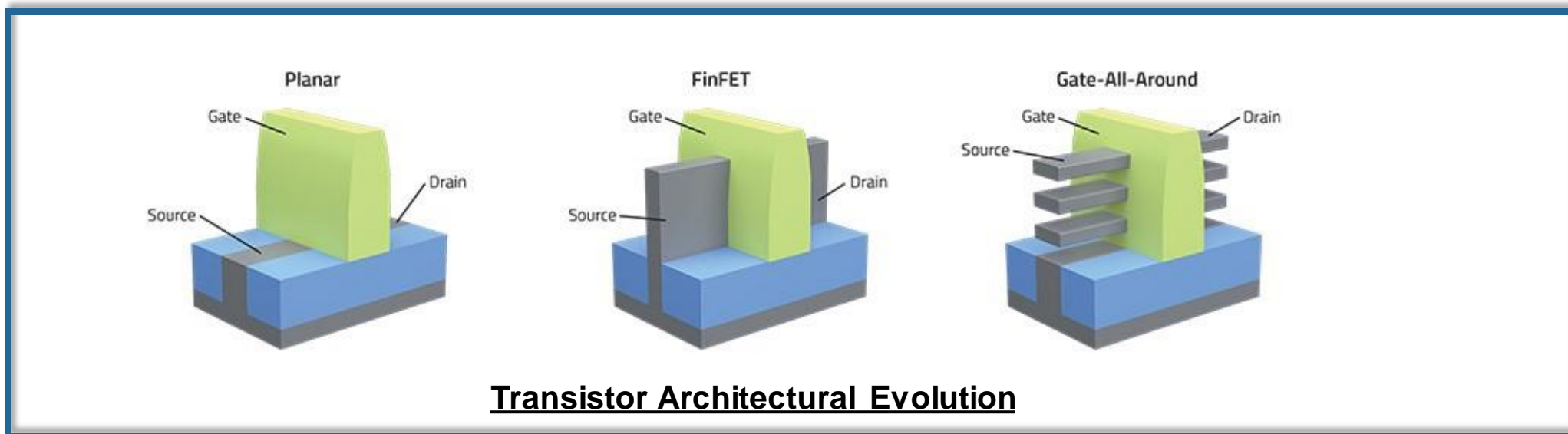
- ▶ **Targets higher voltage (5-40V) product area**
- ▶ **Strong customer demand for solutions**
- ▶ **MST brings significant improvement**
 - Early results showing gains in many areas
 - Allows manufacturers to shrink designs, cut product costs
- ▶ **Early stages of customer rollout**



$L_{\text{DEVICE}} = 1.84\mu\text{m}$

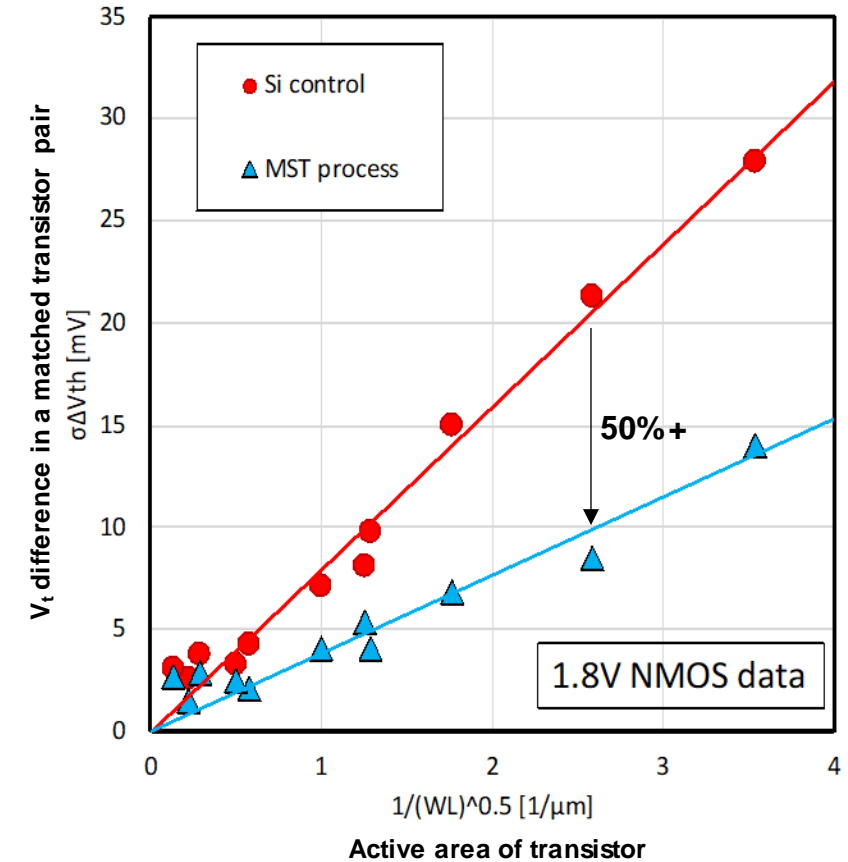
MST: Solving GAA Transistor Challenges

- ▶ Blocks source/drain dopant diffusion
- ▶ Provides enhanced punch-through stop layer between source and drain
- ▶ Lowers contact resistance
- ▶ Reduces HKMG stack height
- ▶ Improves carrier mobility, gate leakage



Variability reduction with MST

- ▶ **High variability between transistors is a significant issue**
 - A big driver of variability is Random Dopant Fluctuation (RDF)
 - Some transistors are designed larger to account for variability
 - This increases costs and limits the minimum achievable voltage and power
- ▶ **Advanced GAA transistor need solutions for RDF**
- ▶ **DRAM sense-amp variability is a major design constraint**
 - Sense-amp margin defines refresh interval and resulting power
 - Improving variability allows smaller sense-amp and reduced power
- ▶ **MST can minimize RDF and lower variability, critical in advanced nodes and memories**



Royalty Opportunity



- ▶ ~410 wafer fabs operating worldwide
- ▶ Adoption of MST in one fab can make Atomera profitable from royalties alone
 - 2023 non-GAAP OPEX guidance is \$16.25M - \$16.75M

| Example 1 Worldwide Average Fab | |
|---|----------------|
| Monthly Fab Capacity ¹ (wafers/month) | 46,240 |
| Industry average wafer ASP - 2018 | \$1,365 |
| Annual Revenue Potential² | \$15.1M |
| Annual Revenue at 50% of ramp ² | \$7.6M |

| Example 2 Leading Foundry, 28nm Fab | |
|---|--------------|
| Monthly Fab Capacity (wafers/month) | 80,000 |
| Industry average 28nm wafer ASP | \$3,300 |
| Annual Revenue Potential² | \$63M |
| Annual Revenue at 50% of ramp ² | \$31.7M |

1. Represents wafers starts per month (200mm equiv) – 227.5M starts in 410 fabs

2. Assumes 2% royalty rate

Source: IC Insights Global Wafer Capacity 2021-2025 report, McClean Report 2021, 2022

MST Customer Business Opportunity



► Foundry economics

| | Wafer Price | GM% | GM\$ Increase | MST Royalty | Wafer Cost | |
|------------------------|-------------|-------|---------------|-------------|------------|--|
| 28nm HP wafer | \$ 3,300 | 45% | \$ - | \$ - | \$ 1,815 | |
| 28nm HP+ wafer | \$ 3,450 | 45% | \$ 68 | \$ - | | 5% higher price for +15% performance boost |
| 28nm HP wafer with MST | \$ 3,600 | 47.0% | \$ 208 | \$ 72 | \$ 1,907 | 30% performance boost=10% higher price (+ \$20 MST cost) |
| 28nm HP wafer with MST | \$ 3,713 | 48.6% | \$ 318 | \$ 74 | \$ 1,909 | 25% die shrink=12.5% price increase (+ \$20 MST cost) |

- **Gross margin increases by \$200-\$300 per wafer after foundry pays Atomera royalties**

► Fabless semiconductor economics

| | Chip sales/ wafer | GM% | GM\$ Increase | Product ASP | Die/wafer | |
|------------------------|-------------------|-----|---------------|-------------|-----------|--|
| 28nm HP wafer | \$ 9,233 | 50% | \$ - | \$ 4.86 | 2,235 | Baseline business for 30mm ² chip |
| 28nm HP wafer with MST | \$ 12,398 | 59% | \$ 3,165 | \$ 4.86 | 3,001 | Improved financials with 25% size reduction |

- **Sales and profit both increase by over \$3000 per wafer for fabless manufacturer**

► Everyone in the value chain benefits from MST technology

Financial Review



| <u>Income Statement</u> | <u>Three Months Ended</u> | | | | | <u>FY 2023</u> |
|---|---------------------------|-------------------|-------------------|-------------------|--------------------|----------------|
| | <u>3/31/23</u> | <u>6/30/23</u> | <u>9/30/23</u> | <u>12/31/23</u> | | |
| <i>(\$ in thousands, except per-share data)</i> | | | | | | |
| REVENUE | \$ - | \$ - | \$ - | \$ 550 | \$ 550 | |
| Gross Profit | - | - | - | 522 | 522 | |
| OPERATING EXPENSES | | | | | | |
| Research & Development | 3,036 | 3,192 | 3,305 | 2,992 | 12,525 | |
| General and Administration | 1,742 | 1,775 | 1,683 | 1,875 | 7,075 | |
| Selling and Marketing | 389 | 393 | 365 | 452 | 1,599 | |
| TOTAL OPERATING EXPENSES | 5,167 | 5,360 | 5,353 | 5,319 | 21,199 | |
| OPERATING LOSS | (5,167) | (5,360) | (5,353) | (4,797) | (20,677) | |
| Other Income (Expense) | 148 | 208 | 314 | 217 | 887 | |
| NET LOSS | \$ (5,019) | \$ (5,152) | \$ (5,039) | \$ (4,580) | \$ (19,790) | |
| Net Loss Per Share | \$ (0.21) | \$ (0.21) | \$ (0.20) | \$ (0.18) | \$ (0.80) | |
| Weighted average shares outstanding | 23,660 | 24,677 | 25,255 | 25,404 | 24,755 | |
| ADJUSTED EBITDA (NON-GAAP) | \$ (4,220) | \$ (4,310) | \$ (4,292) | \$ (3,765) | \$ (16,587) | |
| ADJUSTED EBITDA PER SHARE | \$ (0.18) | \$ (0.17) | \$ (0.17) | \$ (0.15) | \$ (0.67) | |
| <u>Balance Sheet Information</u> | | | | | | |
| Cash, equivalents & ST investments | \$ 17,052 | \$ 23,835 | \$ 20,389 | \$ 19,531 | \$ 19,531 | |
| Debt | - | - | - | - | - | |

Summary

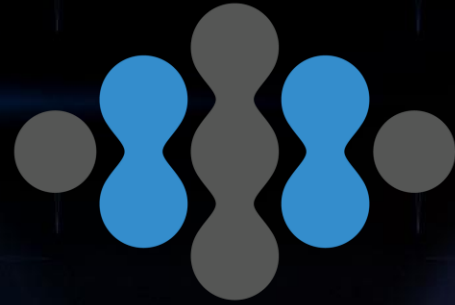


- ▶ High margin, recurring revenue financial model
- ▶ Strong technology, patent position, and balance sheet
- ▶ Traction with many top industry players and growing licensee base
- ▶ Ramping commercial license revenues



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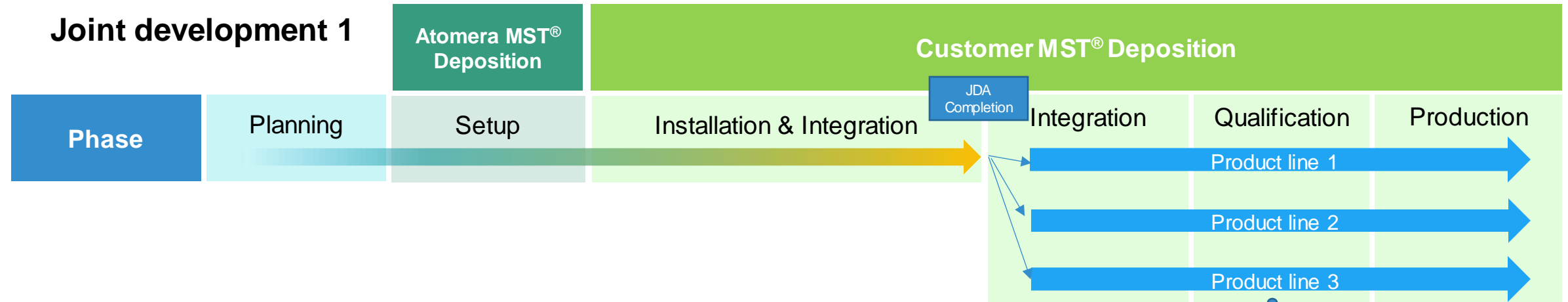
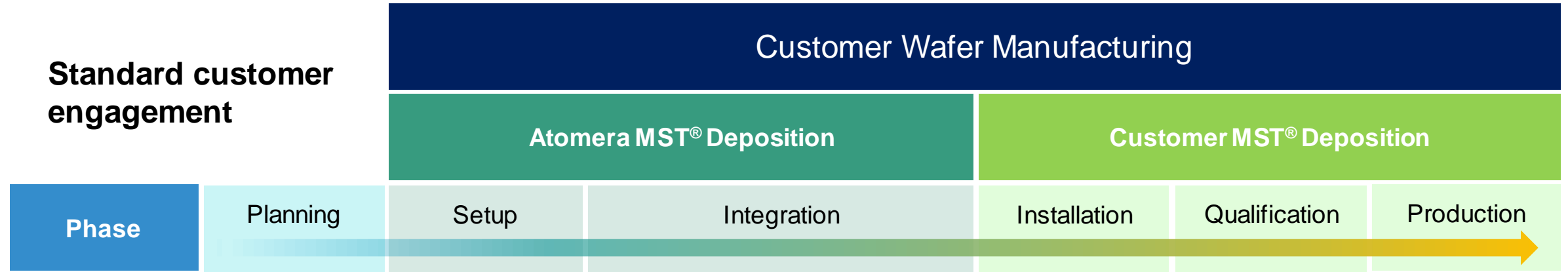
Thank You



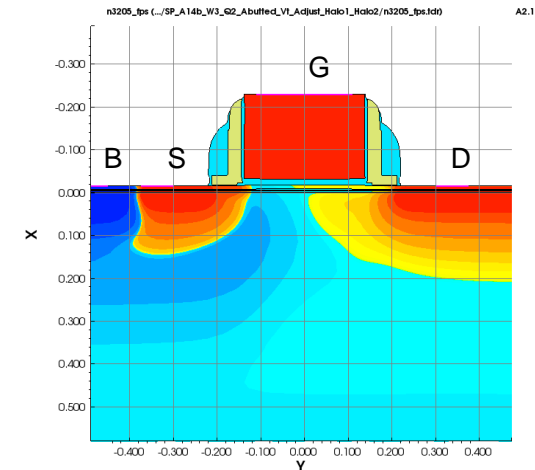
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Backup Slides

Customer Engagement Model



- ▶ **MST-SP is a highly-engineered asymmetric power device**
 - Uses MST to enhance I_{dlin} and precisely control dopant profiles
- ▶ **Improves 5V power devices**
 - Lower R_{SP}
 - Can be traded for up to 20% smaller area
- ▶ **Targeted for rapidly-growing PMIC market**



5V Transistors – Critical and Growing Market



- ▶ **Targeted at rapidly-growing PMIC (Power Management IC) market**
 - Power devices can be up to 80% of PMIC die area
- ▶ **All ICs need stable, regulated power**
 - Across battery charge level, lifetime degradation, and load
 - Across usage modes – DVS (Dynamic Voltage Scaling), sleep, others
- ▶ **5V transistor required to deliver IC power from any source**
 - Battery-powered, USB, wall connected
- ▶ **5V devices do not scale with Moore’s Law**
- ▶ **MST SP allows significant scaling of gate length, and a performance boost**

THE WALL STREET JOURNAL.

“A typical 5G smartphone can hold as many as eight power-management chips, compared with two to three in a 4G phone, according to Hui He, an analyst at research firm Omdia.”

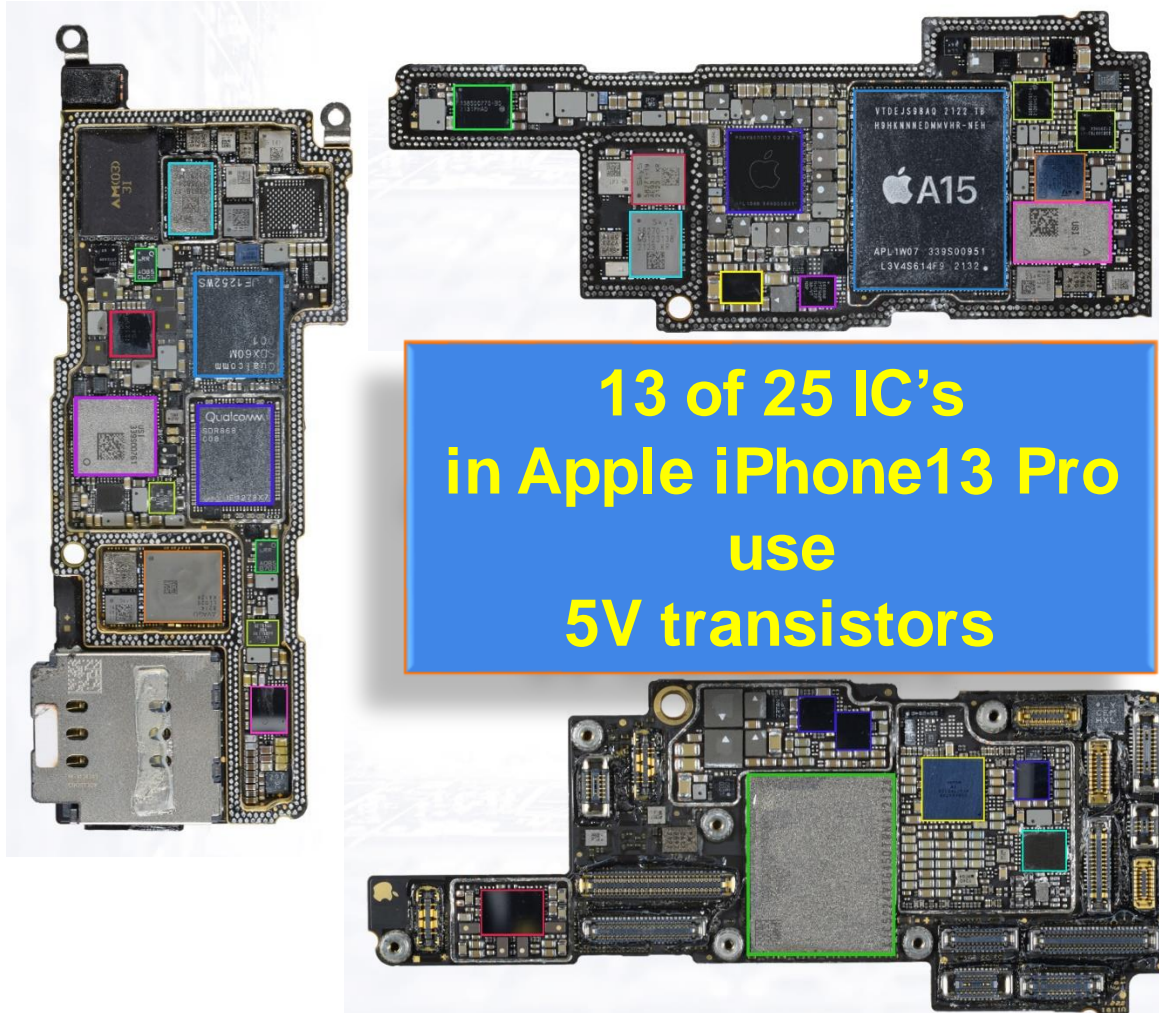
WSJ “Why the Chip Shortage is So Hard to Overcome” 4/20/2021

2018-2025F IC Market Forecast by Device Type (Analog)

| Product Category | 18 | 19 | 19/18 % Chng | 20 | 20/19 % Chng | 21F | 21/20 % Chng | 22F | 22/21 % Chng | 23F | 23/22 % Chng | 24F | 24/23 % Chng | 25F | 25/24 % Chng | 20-25 CAGR |
|------------------------|--------|--------|-----------------|--------|-----------------|--------|-----------------|--------|-----------------|---------|-----------------|---------|-----------------|---------|-----------------|---------------|
| Power Management (\$M) | 14,529 | 14,050 | -3% | 14,640 | 4% | 18,153 | 24% | 20,332 | 12% | 22,568 | 11% | 23,019 | 2% | 24,861 | 8% | 11% |
| Units (M) | 69,243 | 67,227 | -3% | 68,409 | 2% | 80,788 | 18% | 91,396 | 13% | 102,475 | 12% | 105,580 | 3% | 115,178 | 9% | 11% |
| ASP (\$) | \$0.21 | \$0.21 | 0% | \$0.21 | 2% | \$0.22 | 5% | \$0.22 | -1% | \$0.22 | -1% | \$0.22 | -1% | \$0.22 | -1% | 0% |

Source: IC Insight’s McClean Report, June 2021

Example: Use Of 5V Transistor In Apple iPhone13



- Qualcomm Snapdragon X60 5G Modem
- Qualcomm RF Transceiver
- USI Wi-Fi/BT Wireless Combo Module
- Qualcomm PMX60 PMIC
- STMicroelectronics Secure MCU/eSIM
- Qorvo Envelope Tracker IC (2 pcs, likely)
- Qualcomm Envelope Tracker IC
- Avago Front-End Module
- Broadcom Wireless Charging Receiver IC

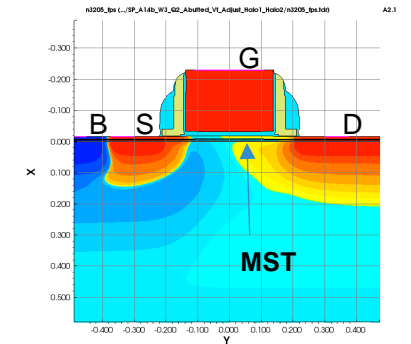
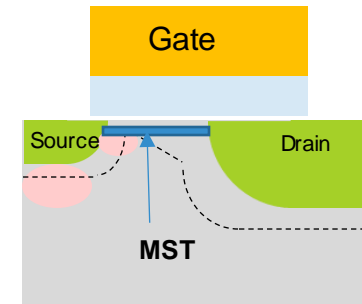
- Apple APL1W07 A15 Bionic PoP (A15 AP + SK hynix 6GB LPDDR4X SDRAM)
- Apple APL1098 PMIC
- NXP Display Port Multiplexer
- Skyworks SKY58271-19 Front-End Module
- Skyworks SKY58270-17 Front-End Module
- Apple/Dialog Semi 338S00770-B0 PMIC
- Apple/Dialog Semi 338S00762-A1 PMIC
- STMicroelectronics STB601A05 PMIC
- USI Apple U1 UWB Module
- Texas Instruments TPS65657B0 Display Power Supply
- KIOXIA 256 GB NAND Flash
- Apple/Cirrus Logic Audio Codec
- NXP SN210 NFC & Secure Element
- Apple/Cirrus Logic Audio Amplifier
- Apple/Cirrus Logic Power Conversion

- iPhone 13 Pro teardown by Tech Insights
- 5V transistor assessment by Atomera

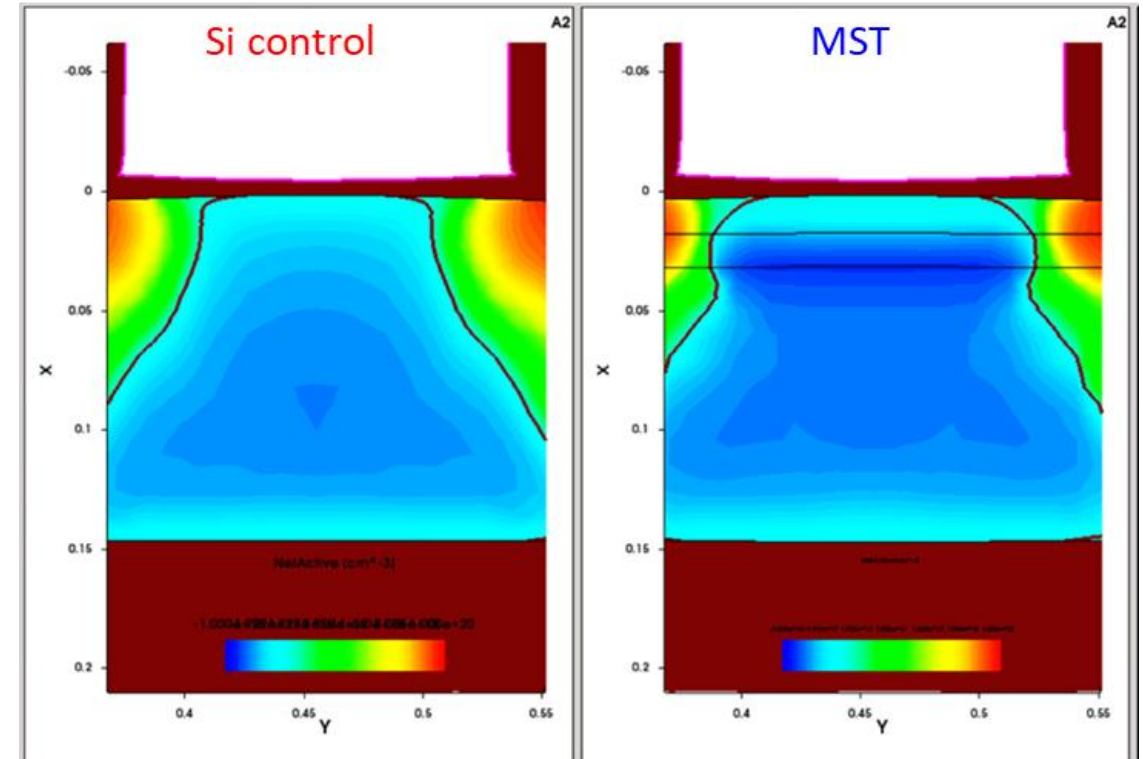
Reference https://www.techinsights.com/blog/teardown/apple-iphone-13-pro-teardown?utm_source=Prospect+Email&utm_medium=Email&utm_campaign=2021+-+Q3+-+Teardown+-+Blog+-+Apple+iPhone+13

5V MST-SP Product – Value Proposition

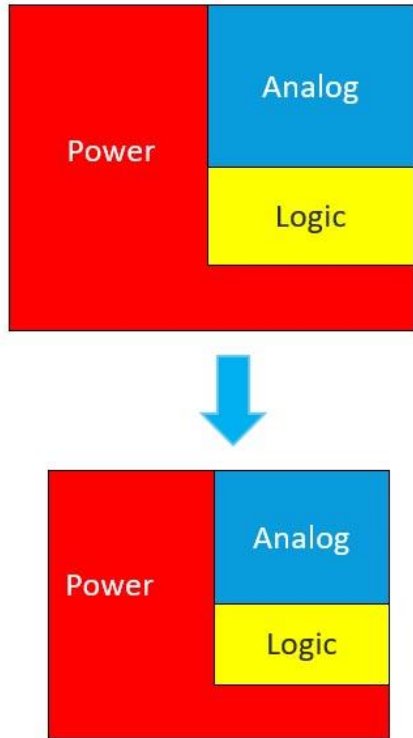
- ▶ **Industry best performance at 180nm (Rsp)**
 - Based on measured silicon data
 - Scalable to smaller process nodes
- ▶ **Meets all reliability requirements**
 - Breakdown Voltage (BVDSS) > 10.5V
- ▶ **Significant cost savings, performance benefits**
 - Die area reduction up to 20%
- ▶ **Demonstrates the big advantage MST can bring to highly optimized designs**
- ▶ **Complete design package accelerates time to production**



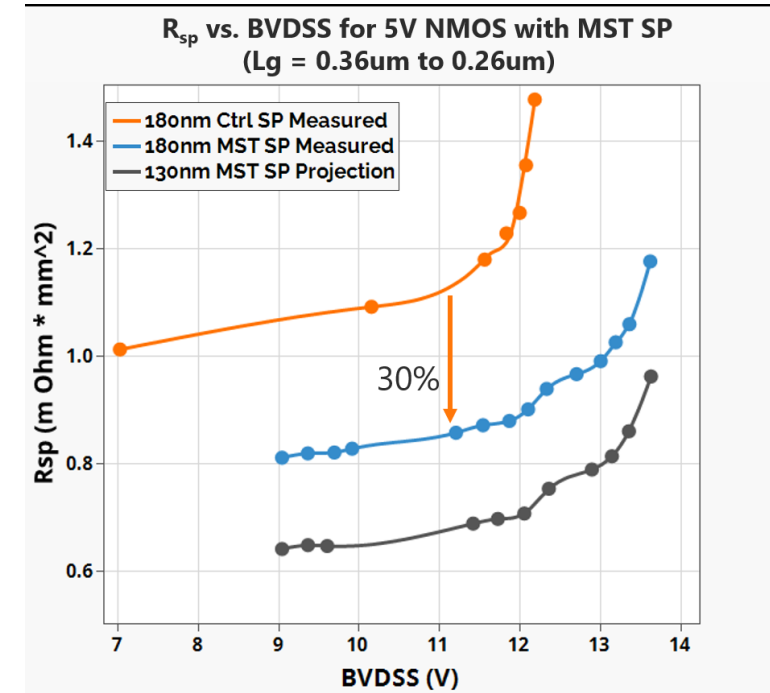
- ▶ **Leading semiconductor companies use TCAD to model manufacturing processes**
 - MSTcad is an add-on for MST
- ▶ **MSTcad can speeds up the time needed to evaluate multiple MST integration options**
- ▶ **Lowers cost of MST evaluation**
- ▶ **Speeds time to successful wafer runs**
- ▶ **Fewer wafer runs lead to faster production**



MST enables legacy capacity expansion

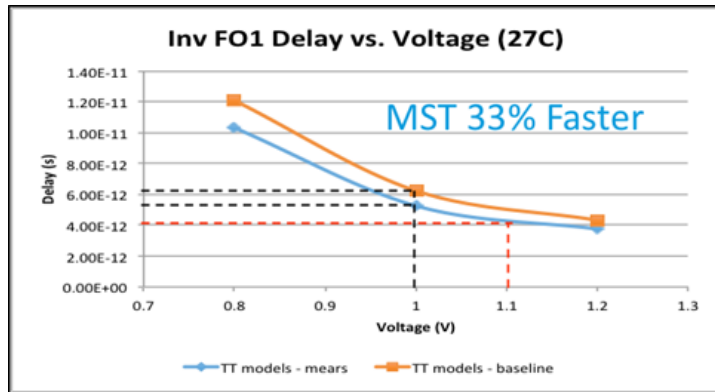


- ▶ **MST provides 30% performance advantage**
 - 0.13u analog design
 - MST vs control silicon
- ▶ **Enables a die shrink of 15-20%**
- ▶ **Smaller die means more manufacturing capacity**
 - Without the cost of building a new fab



MST 28nm benefits

MST shows 30% higher performance



MST performance improvement due to:

- Higher electron mobility
- Improved gate oxide integrity enabling higher overdrive

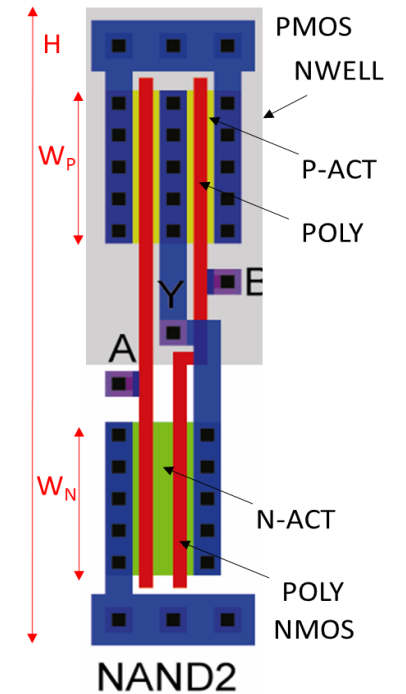
▶ **Performance improvements due to MST can be traded for area reduction**

▶ **28nm PDK SPICE model used to showcase:**

- Logic scaling with MST shows 22-25% area reduction
 - Using a NAND2 gate
- Analog scaling with MST shows up to 21% area reduction

▶ **Implementation of MST on new 28nm designs can result in >20% more production capacity**

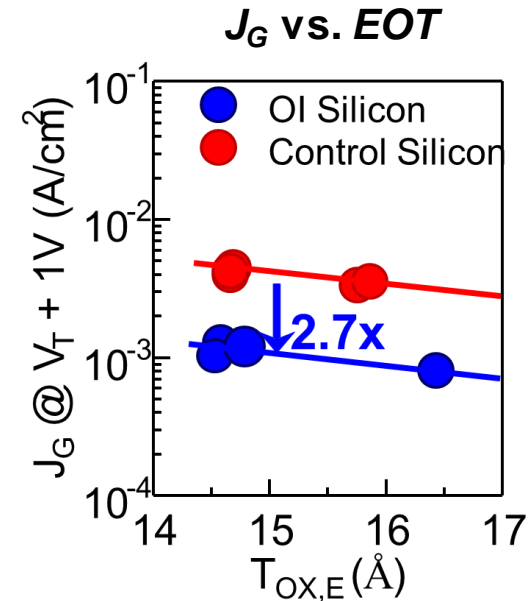
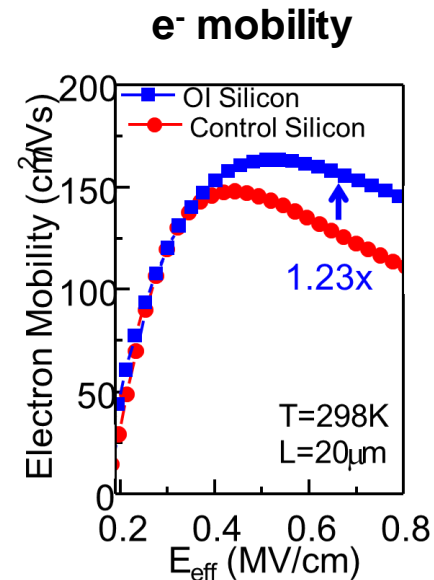
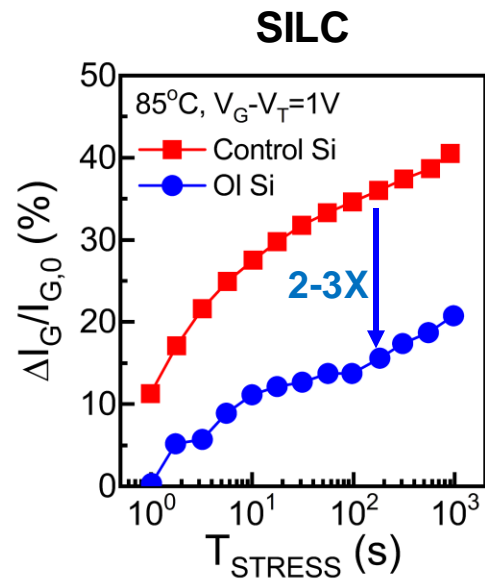
▶ **Allows excellent economic benefits for the whole value chain**



MST for High-k metal gate (HKMG) transistors

► MST enhances HKMG transistor performance and reliability*

- Reduced stress induced leakage current (SILC) enabling reliability improvement
- 23% long-channel mobility enhancement
- 2.7x lower gate leakage

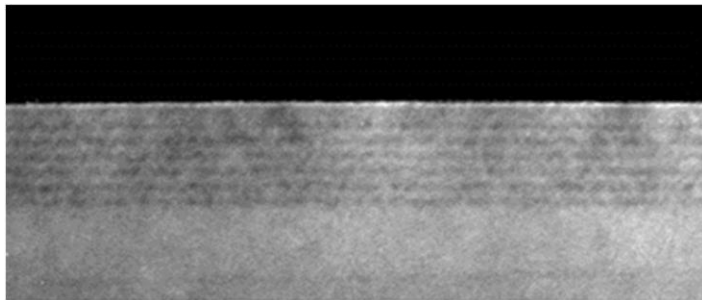


* Professor Suman Datta Group



Quantum Engineered Silicon

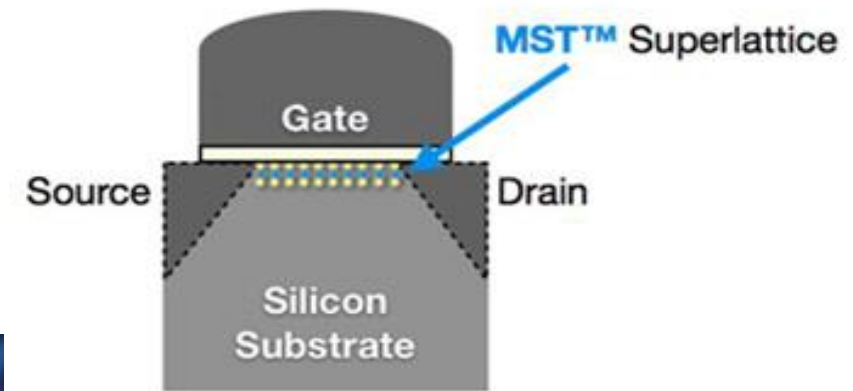
Partial Monolayers of Oxygen in Silicon

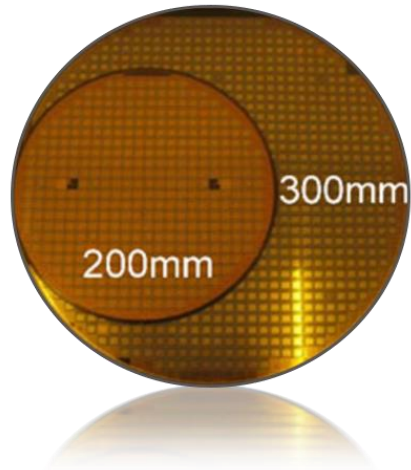


Supported by
Major Semiconductor
Tool Suppliers



MST Enhanced Transistors





Epi Deposition Tool

▶ Epi deposition facility

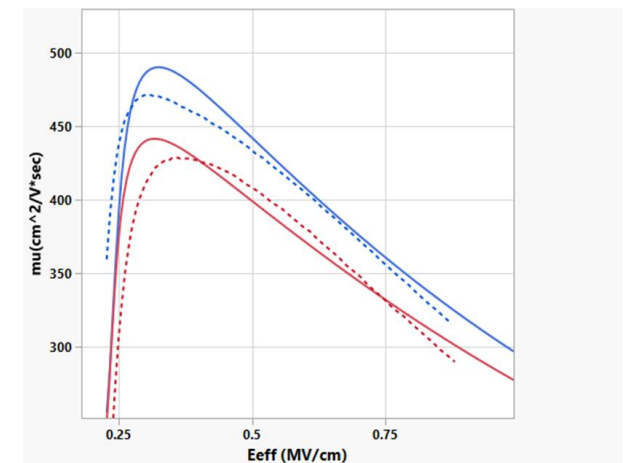
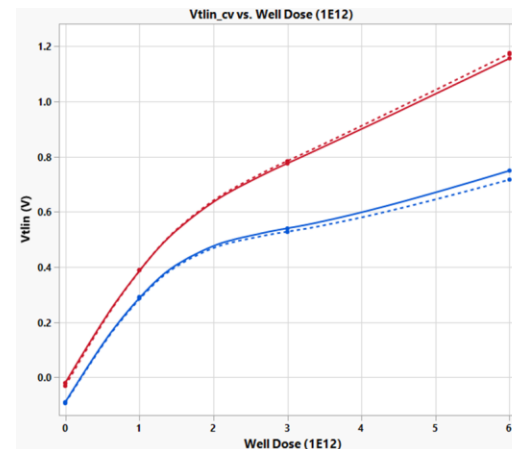
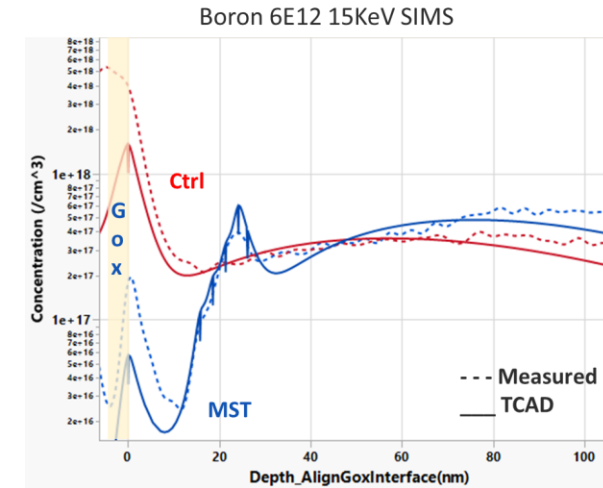
- 300mm Epi deposition
- 200mm Epi deposition
- Wafer cleaning equipment
- Metrology tools
- Advanced wafer handling
- World class clean room facility

▶ Available to deliver customer wafers

Atomera MSTcad™ Progress



- ▶ Leading semiconductor companies use TCAD
- ▶ MST is modelled with a TCAD add-on called MSTcad
- ▶ These plots show silicon verification of MSTcad simulations
- ▶ Enables good electrical match-up for 5V NMOS and MST SP
- ▶ Should speed time to successful results with customers



MST1 vs MST2

▶ MST1

- Blanket technology
- Easy to integrate
- Deposited at beginning of mfg process
- Degraded by high heat in STI/Well module
- Faster time to market for low heat processes
- Used for FinFET, RFSOI, newer process nodes

▶ MST2

- Selective technology
 - Integrated after STI/Well so avoids highest heat
- More flexible to apply to selected areas only
- Used for 5V, Analog, older process nodes

Wafer manufacturing process

Blank Si wafer

Shallow Trench Isolation (STI) & Well module

Gate module

Source/Drain module

MST1

MST
Si

STI MST STI
Si

STI S Gate MST D STI
Si

MST2

Si

STI Si STI

STI MST STI
Si

STI S Gate MST D STI
Si